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A THREE STAGE COMPARATOR AND ITS MODIFIED VERSION WITH HIGH SPEED AND LOW NOISE

Dr. G.Padma Priya[1], Aramati Ashok Reddy[2], Adiandhra Nagaseshu[3], Gulladurthi Sujana Sree[4], Dhara Leela Krishna[5], E Guna Sai[6]

[1]*Associate Professor, Dept. of ECE, S V College of Engineering, Tirupati, A.P, India.*

[2,3,4,5,6]*B. Tech Student, Dept. of ECE, S V College of Engineering, Tirupati, A.P, India.*

ABSTRACT

In this paper we are proposing modified version of three-stage comparator to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the proposed three-stage comparator has an extra amplification stage, which increases the voltage gain and the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator make use of nMOS input pairs in both the regeneration stage and the amplification stage. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. This greatly reduces the kickback noise by canceling out the nMOS kickback through the pMOS kickback. It also adds an extra signal path in the regeneration stage, which helps increase the speed further. For easy comparison, both the proposed and the modified three stage comparators are implemented in the same 45nm CMOS process.

Keywords: *Kickback Noise, Amplification stage, Regeneration stage.*

INTRODUCTION

The need for ultra-low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. Nowadays, many applications involve digital signals and processing. Designers of digital integrated circuit (IC) need to develop a fast analog to digital converter (ADC) circuit because ADC will influence the overall performance of the applications. In these applications, the power consumption and processing time is very critical [1]. Most ADCs use a comparator as a part of their building blocks. Hence the comparator must have a high speed and consume less power. Comparator is used to compare two signals and give the output based on the comparison. Since the input signals are usually low in amplitude, a preamplifier circuit is needed for the comparator. A differential amplifier with active loads is usually the first stage of the preamplifier. The differential amplifier will produce a very high gain. It amplifies the difference between two input voltages. The output of the preamplifier is connected to the decision-making circuit or latch. A preamplifier based comparator is a regenerative comparator; it uses back to back latch stage and positive feedback. A latch is defined as the memory unit that stores a charge on the gate capacitance of an inverter. A commonly used architecture in analog circuits is a

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dynamic latch because it provides excellent speed along with an acceptable accuracy. The latch works in two phases which is governed by a clock (CLK) level either low or high.

EXISTING METHOD

Static comparators have been used in the past; however, they are impractical for portable applications because of their limited speed and significant amounts of power consumption. One-stage dynamic comparators were proposed to reduce the power consumption and improve the speed [2]. In paper [3], a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages.

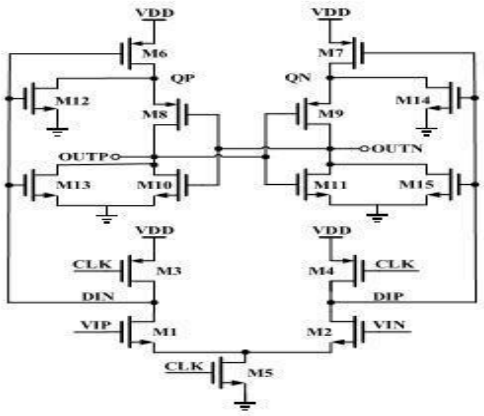

Fig. 1: Miyahara's two stage comparator [4]

Fig. 1 shows the Miyahara's two-stage comparator, which has the limitation of pMOS input pair in the latch stage which limits the regeneration speed due to reduced hole mobility [5]. Although the Miyahara's two-stage comparator increases the speed, its speed can be further improved by using nMOS transistors in the latch input pair, so that the regeneration speed can be improved.

PROPOSED METHOD

In the three stage comparator, three stages are connected one after another. Compared with the

Miyahara's comparator, the major difference is that one extra preamplifier is added. This extra preamplifier acts as an inverter, and makes the latch stage able to use nMOS input pair instead of pMOS input pair, which leads to increased speed. The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise. After the first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair to have a large gate–source voltage equal to VDD. As a result, the current is large enough for quickly pulling up RP and RN. This means that the extra delay incurred by the second stage is small compared to the large delay of the latch stage.

Furthermore, compared to the first-stage output load in the Miyahara's comparator, the first stage output load in the three stage comparator. The output load is reduced by several times, improving the amplification speed.

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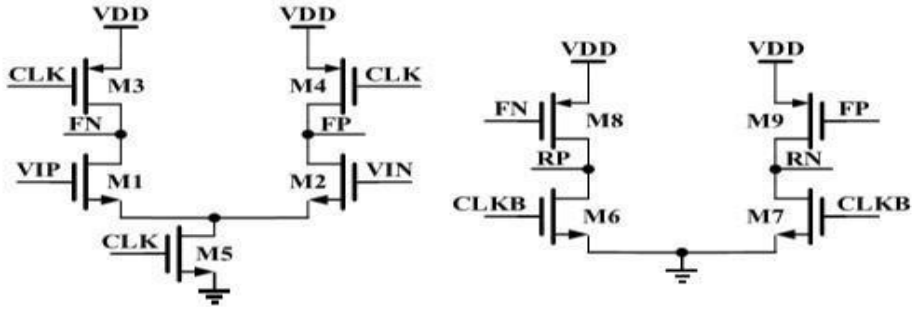
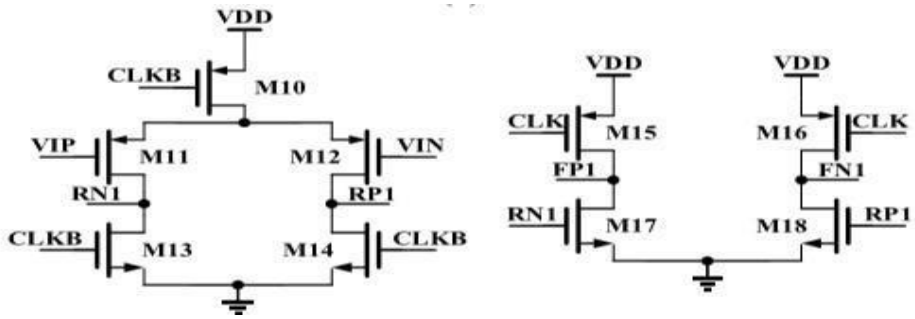
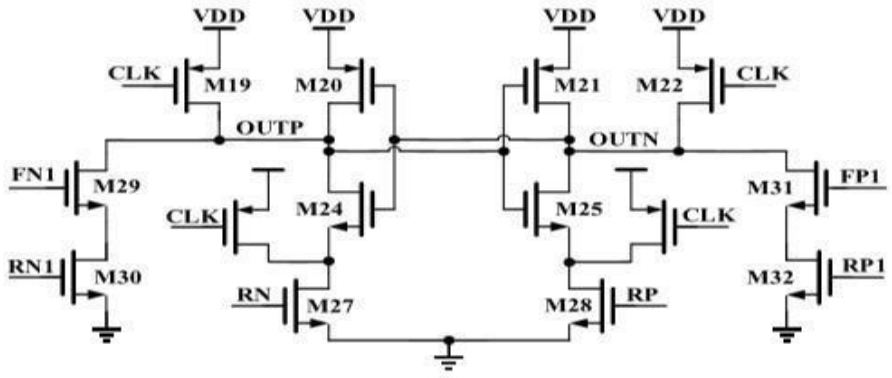
In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of three-stage comparator, as shown in Fig. 4. Compared to the original version in the previous section, the only difference is that the modified version has the extra first two stages of Fig. 4(b) and extra paths M29–32 in the latch stage of Fig. 4(c). The extra first two stages use pMOS input pair.



(a)



(b)



(c)

Fig 4: Proposed modified version of three stage comparator (a) first two stages with n-MOS input pair. (b) Extra two stages with p-MOS input pair. (c) Latch stage (Third stage).

M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29– 32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further, and the input

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referred offset and noise are suppressed further. The operation of these extra circuits is as follows. In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 in Fig. 4(b) are reset to GND, while FP1 and FN1 are reset to VDD. This turns off M30 and M32 in Fig. 4(c), ensuring that there is no static current in the extra path M29–32.

In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 in Fig. 4(b) rise to VDD (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). Because the rising of RP1 and RN1 occurs before the falling of FP1 and FN1, the extra paths in Fig. 4(c) are turned on for a limited time, drawing a differential current from the latching nodes OUTP and OUTN. This generates a differential voltage at OUTP and OUTN, which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths in Fig. 4(c) are turned off again to prevent the static current

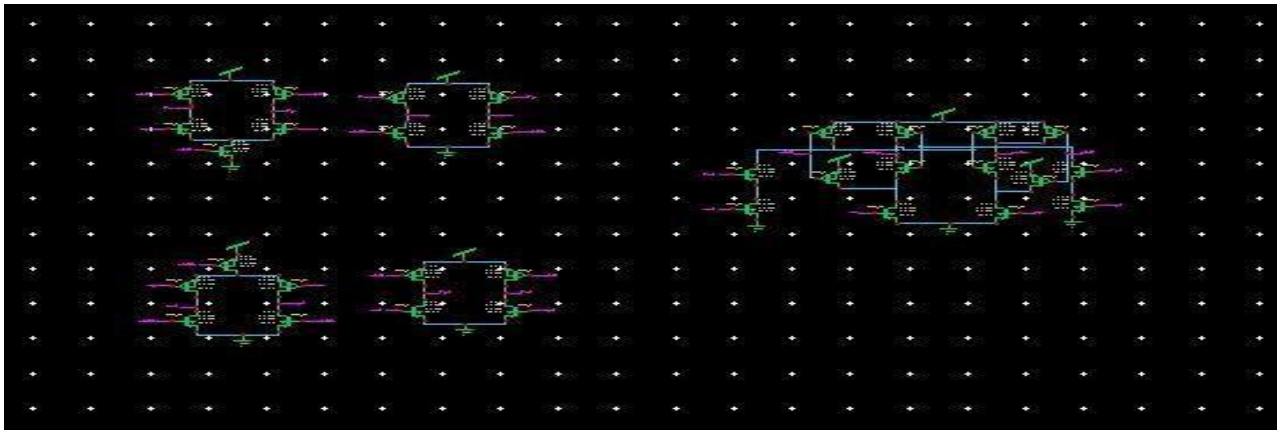
Overall, the modified version of three-stage comparator has the advantages of faster speed, lower input referred offset and noise.

METHODS USED

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.0. The features and functionality of this tool has been described below:

- Schematic Editor (S-Edit): Schematic editor is a powerful design capture and analysis package that can generate netlist directly usable in T-Spice simulations.
- T-Spice Circuit Simulator: T-Spice performs fast and accurate simulation of analog and mixed analog/digital circuits.
- Waveform Editor (W-Edit):W-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.
- Layout Editor (L-Edit): Tanner EDA tool includes L-Edit for layout editing.

RESULTS AND DISCUSSION



Schematic diagram proposed modified comparator

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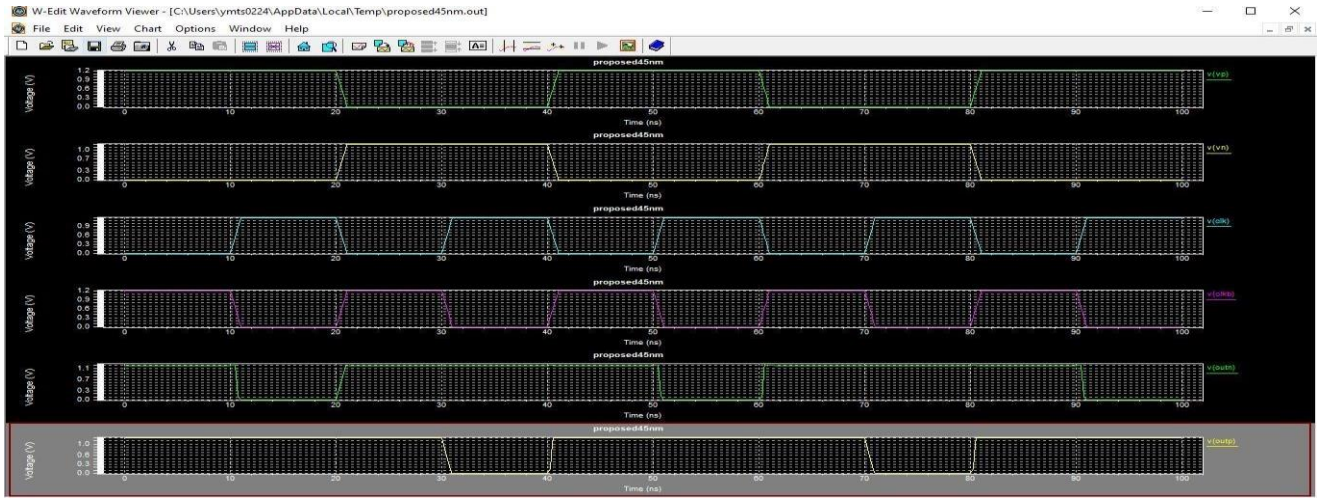

Waveform of proposed modified comparator

Table: 1 Evaluation of power, delay, area parameters

	DELAY (ns)	POWER (uW)
EXISTING	1.1	1.7
PROPOSED	0.6	3.1

ADVANTAGES

- In the proposed method, The extra first two stages use pMOS input pair M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further.

DISADVANTAGES

- Large power consumption

APPLICATIONS

There are several applications of Comparator

- They are used in Audio/Video devices.
- They are used in Cell Phones.
- They are widely used in CMOS Image sensors for mobile applications.

CONCLUSION

This paper presents a three-stage comparator and its modified version, which have the advantages of fast speed, low kickback noise. These comparators are well suited for high-speed high resolution SAR ADCs. All the circuit designs are implemented in Tanner EDA tool in 45 nm technology.

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FUTURE SCOPE

By applying low power techniques for the proposed comparator architecture, the static power consumption which is the major concern can further be reduced.

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